

We claim:

1. A method of producing a packetized signal comprising:
 - (a) receiving a plurality of input signals;
 - 5 (b) buffering each of the input signals in a memory system;
 - (c) processing at least one of the input signals to provide a processed signal and buffering the processed signal in the memory system;
 - (d) designating at least some of the input signals or the processed signals as packet source signals and assigning each of the packet source
10 signals a unique global identification code;
 - (e) retrieving at least one of the packet source signals and generating the packetized signal wherein the packetized signal includes a series of packetized signal packet, wherein each of the packetized signal packets contains the global identification code of one of the packet source
15 signals and data corresponding to the same packet source signal.
2. The method of claim 1 wherein each of packet source signals comprises a series of packet source signal packets, and wherein each of packetized signal
20 packets is formed by retrieving one or more the packet source signal packets corresponding to a single packet source signal, extracting data from the retrieved packets, recording the global identification code of the single packet source signal and at least a portion of the extracted data in the packetized signal packet.
3. The method of claim 1 wherein each of packet source signals comprises a
25 series of packet source signal packets, and wherein each of packetized signal packets is formed by retrieving one or more the packet source signal packets corresponding to a single packet source signal and including the packet source signal packet within the packetized signal packet.
- 30 4. The method of claim 1 wherein each of packetized signal packets includes a global identification code, packet sequencing information and a data payload.

5. The method of claim 4 wherein the single packet source signal is a video signal and wherein each packetized signal corresponding to the packet source signal includes video data and position information indicating how the video data is to be displayed on a video display.

6. The method of claim 5 wherein the position information includes pixel information indicating a position within a window at which the video data is to be displayed.

7. The method of claim 1 wherein the processing step includes scaling one of the input signals to provide a processed signal.

8. The method of claim 1 wherein the processing step includes compressing one of the input signals to provide a processed signal.

9. A method of producing one or more output signals, the method comprising:

- (a) receiving a plurality of input signals;
- (b) buffering each of the input signals in an input processor memory system;
- (c) processing at least one of the input signals to provide a processed signal and buffering the processed signal in the memory system;
- (d) designating at least of the input signals or the processed signals as packet source signals and assigning each of the packet source signals a unique global identification code;
- (e) retrieving at least one of the packet source signals and generating the packetized signal wherein the packetized signal includes a series of packetized signal packet, wherein each of the packetized signal packets contains the global identification code of one of the packet source signals and data corresponding to the same packet source signal;
- (f) transmitting the packetized signal across a communications link;

- (g) receiving the packetized signal;
- (h) extracting each of the packetized signal packets from the packetized signal;
- (i) buffering each of the packetized signal packets containing the same global identification code in a separate data buffer in an output processor memory system and designating the packetized signal packets in each separate data buffer as an output source signal;
- (j) producing each of the output source signals by retrieving one or more output source signals and combining the retrieved output source signals.

10. The method of claim 9 wherein each of packet source signals comprises a series of packet source signal packets, and wherein each of packetized signal packet is formed by retrieving one or more the packet source signal packets corresponding to a single packet source signal, extracting data from the retrieved packets, recording the global identification code of the single packet source signal and at least a portion of the extracted data in the packetized signal packet.

11. The method of claim 10 the single packet source signal is a video signal and wherein each packetized signal corresponding to the packet source signal includes video data and position information indicating how the video data is to be displayed on a video display.

12. The method of claim 9 wherein the processing step includes scaling one of the input signals to provide a processed signal.

13. The method of claim 9 wherein the processing step includes compressing one of the input signals to provide a processed signal.

14. A system for receiving a plurality of input signals and for producing a plurality of output signals, the system comprising:

- (a) a master controller for generating input processor control signals and output processor control signals;
- (b) an input processor having:
 - (i) a plurality of input ports for receiving the input signals;
 - 5 (ii) a plurality of input signal processors for processing the input signals to provide processed signals
 - (iii) an input processor memory system for buffering the input signals and the processed signals, wherein at least some of the buffered signals are designated as packet source signals;
 - 10 (iv) a packetized signal output port;
 - (iv) one or more packetized signal output stages for retrieving one or more packet source signals from the input processor memory system and for producing a packetized signal at the packetized signal output port, wherein the packetized signal contains data
 - 15 corresponding to each of the retrieved signals; and
 - (v) an input processor local controller for controlling the operation of at least the signal processors and the packetized signal output stages in response to the input processor control signals;
- (c) an output processor having:
 - 20 (i) a packetized signal input port for receiving the packetized signal;
 - (ii) a packetized signal input stage for extracting data corresponding to each of the packet source signals from the packetized signal and for storing data corresponding to each of the packet source signals in a separate buffer in the output processor memory
 - 25 system as an output source signal;
 - (iii) an output signal generator for providing one or more output signals, each of the output signals corresponding to one or more of the output source signals;
 - (iv) and output processor local controller for controlling the operation
 - 30 of packetized signal input stage and the output signal generator in response to the output processor control signals; and

- (d) a communications link coupled between the packetized signal output port and the packetized signal input port.

5 15. The system of claim 14 wherein each of the packetized signal comprises a series of packetized signal packets, and wherein each packetized signal packets contains a global identification code.

10 16. The system of claim 14 wherein the signal processors include one or more video scalers for providing a scaled version of the input signal as a processed signal.

17. The system of claim 14 wherein the signal processors include one or more data compression elements for providing a scaled version of the input signal as a processed signal.

15 18. The system of claim 14 further comprising one or more A/D converters coupled between one or more of the input ports and the input processor memory system.

20 19. The system of claim 17 wherein the data compression elements include one or more horizontal line filters.

20. The system of claim 17 wherein the data compression elements include one or more vertical line filters.

25 21. An input processor comprising:
(a) a plurality of input ports for receiving a plurality of input signals;
(b) a memory system for buffering the input signals;
(c) one or more signal processors for retrieving the input signals from the memory system and for processing the input signals to generate processed signals and for storing the processed signals in the memory
30 system;
(d) an output port;

- (e) a packetized signal output stage for retrieving one or more of the processed signals from the memory system and for generating a packetized signal containing information from the retrieved signals and for providing the packetized signal at the output port; and
- 5 (f) an input processor local controller for controlling the operation of the the memory system, the signal processors and the packetized signal output stage.

22. The input processor of claim 21 wherein the signal processors include one or
10 more video scalers for processing an scaled version of the input signal as a processed signal.

23. The method of claim 24 further comprising a step of processing packetized
15 signal packets corresponding to a particular global identification code to provide a set of processed packets, assigning the set of processed packets a unique global identification code and storing the processed packets in packet storage locations and treating the processed packets as packetized signal packets.

24. A method of generating one or more outgoing packetized signals, the method
20 comprising:

- (a) receiving one or more incoming packetized signals, each of the packetized signals including a plurality of packetized signal packets identified with a global identification code;
- (b) recording each of the packetized signal packets in a packet storage
25 location;
- (c) recording a number of outgoing packetized signals in which each of the packetized signal packets will be included;
- (d) instructing a group of packetized signal output stages to read each of the packetized signal packets, the number of packetized signal output stage
30 corresponding to the number recorded in (c).

25. A packet router comprising:

(a) a plurality of input stages, each of the input stages configured to receive an incoming packetized signal and store packetized signal packets extracted from the packetized signal in a memory system;

5 (b) a plurality of output stages, each of the output stages configured to read packetized signal packets from the memory system and generate an outgoing packetized signal corresponding to the packetized signal packets read by the output stage; and

10 (c) a router controller for controlling the storage of the packetized signal packets in the memory system and the generation of the outgoing packetized signals in response to router control signals received from a master controller.

26. The packet router of claim 25 wherein the memory system includes a plurality
15 of packet storage locations and wherein the router controller includes a storage location table to manage the usage of the packet storage locations and a global identification code distribution table to manage the distribution of packetized signal packets to particular output stages, and wherein the router controller is configured to instruct the input stages to store each packetized signal packet in a free packet
20 storage location and to instruct each of the particular output stages to read the packetized signal packet from the packet storage location.

27. The packet router of claim 25 wherein the global identification code distribution
25 table identifies the particular output stages to which packets having a particular global identification code are distributed.

28. The packet router of claim 25 wherein the storage location table tracks the
number of output stages that require a packetized signal packet from each packet
storage location and identifies a particular packet storage location as free if no output
30 stage requires a packetized signal packet in the particular packet storage location.